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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,012	11/17/2003	Samuli Stromberg	79707	3322

22242 7590 05/19/2005

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EXAMINER	
HESS, DANIEL A	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/715,012	STROMBERG ET AL.	
	Examiner	Art Unit	
	Daniel A. Hess	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9-12,14-17,20,21 and 23-25* is/are rejected.

7)☒ Claim(s) *8,13,18,19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicant's 2/22/2005 amendment and arguments, which have been placed in the file of record. This action is non-final.

Information Disclosure Statement

The information disclosure statement filed 4/21/2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. **Only those foreign patent documents that have been supplied have been considered.**

Response to Arguments

Applicant's arguments filed 2/22/2005 have been fully considered. There appear to be essentially two main thrusts in those arguments.

Firstly, regarding the 112 rejection of claim 4 and related dependent claims that had been made, this rejection is withdrawn because the applicant's argument that was made in the 2/22/2005 response is considered persuasive. Since no art rejection had previously been made with respect to claim 4 and various claims which depended therefrom, **this action is non-final**.

Secondly, regarding arguments relating to relative size of the various substrates and various capacitive plates, the examiner is of the view that to make one of the substrates smaller would have been an obvious extension of the teachings of Seiichi.

Regarding size of the respective substrates, the examiner makes reference to Minoru (US 5,309,326). In Minoru, one substrate containing a chip (see cover figure reference 20) is electrically connected to another substrate containing a chip 21, and the size of the substrate containing the chip is much smaller. In general, a lot of variations can be seen in substrate sizes, and these should not be considered patentable differences.

Also, in Seiichi (see figure 1) the substrate 1A containing the IC chip could clearly be made smaller and still carry all of the elements that are on the substrate 1A, since the substrate 1A has a lot of space around the edges.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 7, 9, 10, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi (JP 2000057287), **of record in the applicant's information disclosure** in view of Minoru (US 5,309,326).

Re claim 1: See especially figure 1(a) – 1(c); see also abstract, which is taken to be a fair representation of the invention. There a circuitry pattern (figure 1b) on a smart label substrate

(ref. 1b). There is a structural part (figure 1a) having an IC. As figure 1(c) shows, layers 1A and 1B are brought together and connected by capacitors 4, 5, and 6 of 1A which form a capacitive electrical connection to corresponding opposite plates 7, 8 and 9, as is well-shown in figure 1(c).

Seiichi fails to show a size disparity between the structural part containing the chip and the substrate to which it is attached.

Minoru teaches (see figure 1) that a smaller substrate 20 containing a chip is attached to a much larger substrate.

In view of Minoru's teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the chip-bearing substrate of Seiichi such that it is smaller, as shown in the teachings of Minoru because this results in a smaller size and lighter weight, often desirable in such cards. Note that in Seiichi (see figure 1) the substrate 1A containing the IC chip could easily be made smaller and still carry all of the elements that are on the substrate 1A, since the substrate 1A has a lot of space around the edges.

Re claim 2: See figure (1b): there are at least two capacitors connected in series located outside of the chip, namely, either 7 and 8 or 7 and 9, which are in series.

Re claim 3: See translation, page 2, [0014]: the intervening layer 10 of figure 1(c) binding the two layers is a thermoplastic layer.

Re claim 6: The type of materials used as substrates in such cards are typically made of plastic and thus are electrically insulating. The claimed dissipation factor is typical of plastics. Plastics are known non-conductors, as evidenced by their use as insulation on wires.

Re claim 7: Polyolefins are not unusual as substrate materials in the art of ic cards and transaction cards. US 6555213 to Koneripalli et al. entitled "Polypropylene card construction" is one of many examples.

One would have been motivated to include such a material because it is sturdy and not electrically conductive.

Re claim 9: The insulating resin 10 of Seiichi could be a thermoplastic. Then the limitation of the claim is met.

Re claim 10: Polyester is a standard and common card material. See for example Clayman et al. (US 6,644,551).

The motives to include polyester include sturdiness, durability and flexibility.

Re claim 14: Polypropylene and polyethylene are common plastics used in cards. The motive is flexibility and durability.

Claims 11, 12, 15, 16, 20, 21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi as modified by Minoru (US 5,309,326) in view of Asplund (US 6,293,470). The teachings of Seiichi have been discussed above.

Re claims 11, 12: Seiichi teaches the final recited product in claim 1, but fails to teach the means of attachment by carrier web.

Asplund teaches (see especially figures 3 and 4) bringing layers together via carrier webs that deliver various components that are then brought together.

In view of Asplund's teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the old and well-known carrier webs to deliver

components that are then brought together because this can result in faster and cheaper production.

Re claim 15: See discussion re claim 11 above, and note that examiner's position that the sizes of the different substrates are not critical has been discussed above.

Re claim 16: See discussion re claim 2, above.

Re claim 20: See discussion re claim 6, above.

Re claim 21: See discussion re claim 7, above.

Re claim 23: See discussion re claim 3, above.

Re claim 24: See discussion re claim 9, above.

Re claim 25: See discussion re claim 10, above.

Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi/Minoru as applied to claim 1 above, in view of Kasuga et al. (US 2003/0209392).

Seiichi/Minoru fails to teach or fairly suggest the use of an anisotropic conductive film in the smart label.

Kasuga et al. (US 2003/0209392) teaches (paragraphs 29, 33, 60, 64 and 65) the use of an anisotropic film in a smart label.

In view of Kasuga et al's teachings, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the old and well-known anisotropic film of Kasuga et al. among the layers of Seiichi/Minoru because thereby one can avoid wire bonding wherever wires would be bonded, which involves risk of damaging the circuit.

Allowable Subject Matter

Claims 8, 13, 18, 19, 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Re claims 8, 18, 19, 22: In the context of the various limitations upon which the claim depends, there is no teaching or motivation found in the prior art of record that the structural part is attached to the smart label substrate on the side opposite to the side where the circuitry pattern is located, and the dielectric layer is the smart label substrate.

Re claim 13: In the context of the various limitations upon which the claim depends, there is no teaching or motivation found in the prior art of record for the recited printed isolation layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel A Hess whose telephone number is (571) 272-2392. The examiner can normally be reached on 8:00 AM - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAG.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAG system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DH

5/6/05

DANIEL STCYR
PRIMARY EXAMINER